TRANSISTOR IGBT AND MOSFET DRIVER DR2180P–B1
ANALOGUE of 2SD315AI

USER'S MANUAL

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1 OVERVIEW

Double-channel driver of powerful transistors with field drive (MOSFET or IGBT) (hereinafter – driver) is intended for dependant galvanic isolated control of two power transistors with maximum permissible voltage up to 3300 V. The driver is an amplifier – generator of transistor gates control signals with frequency up to 100 kHz. The driver contains built-in galvanic isolated DC/DC-converter, providing requisite levels of unlocking and locking voltages on transistor gate. The driver is an analogue of **2SD315AI** in structure and function.

2 DRIVER COMPOSITION

2.1 The driver is a printed-circuit board with installed driver module on it (DM), made in hermetic plastic housing, necessary tuning element and connectors for connection of controlled transistors and control signals.

2.2 The driver contains the following functional assemblies:

1 Driver supply voltage stabilizer with protection against false turn-on polarity;
2 Built-in DC-DC converter with stabilization of unlocking and locking voltage levels on gates of controlled transistors;
3 Input logic;
4 Drive circuit of controlled transistor gates;
5 Protection circuit against undervoltage and over-voltage on controlled transistors gate;
6 Protection circuit of controlled transistors against current overload.

3 FUNCTIONAL DRIVER FEATURES

3.1 The driver provides the following driving functions, controlling and protecting functions of controlled transistor:

1 Saturation voltage control on collector-emitter of controlled transistor, its protective disconnection when saturation state output;
2 Threshold regulation of protective turn-off on saturation voltage;
3 Smooth driver junction from active state to inactive one when “emergency” (output of controlled transistor from saturation mode);
4 Control block when “Emergency”;
5 Emergency signaling;
6 On/off time regulation of controlled transistor by means of change of resistor resistance in output circuit (Ron, Roff);
7 Block of simultaneous turn-on of upper and lower arm;
8 Switching delay of upper and lower arm;
9 Switching delay regulation of upper and lower arm;
10 Driver supply voltage control (built-in comparators) on DC/DC converter output.

3.2 Overall drawing is shown at Figure 1, functional driver scheme is represented at Figure 2

* It is necessary to use additional diodes, see Section 6, paragraphs C1, C2.

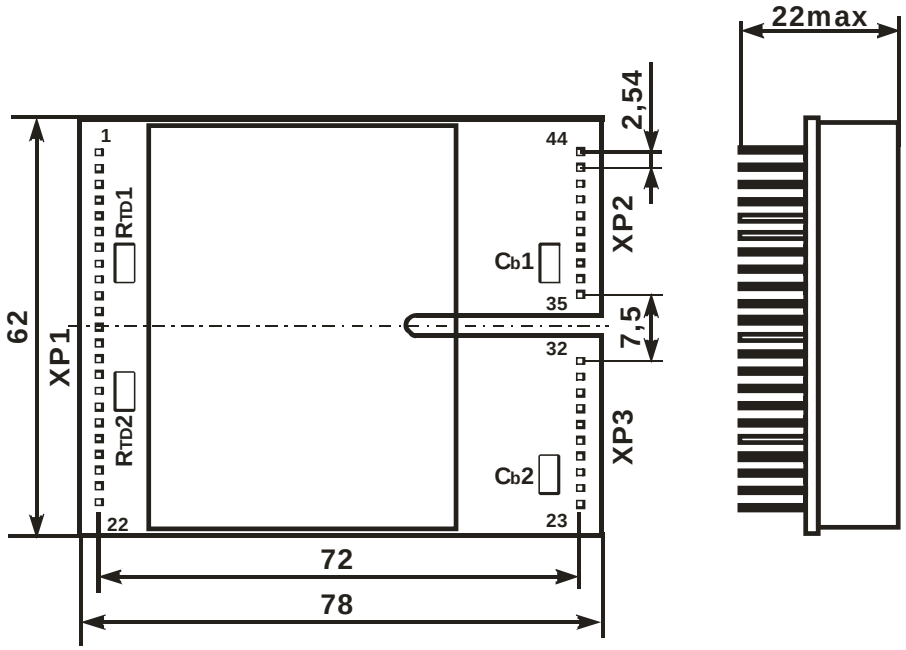


Figure 1 – Overall drawing

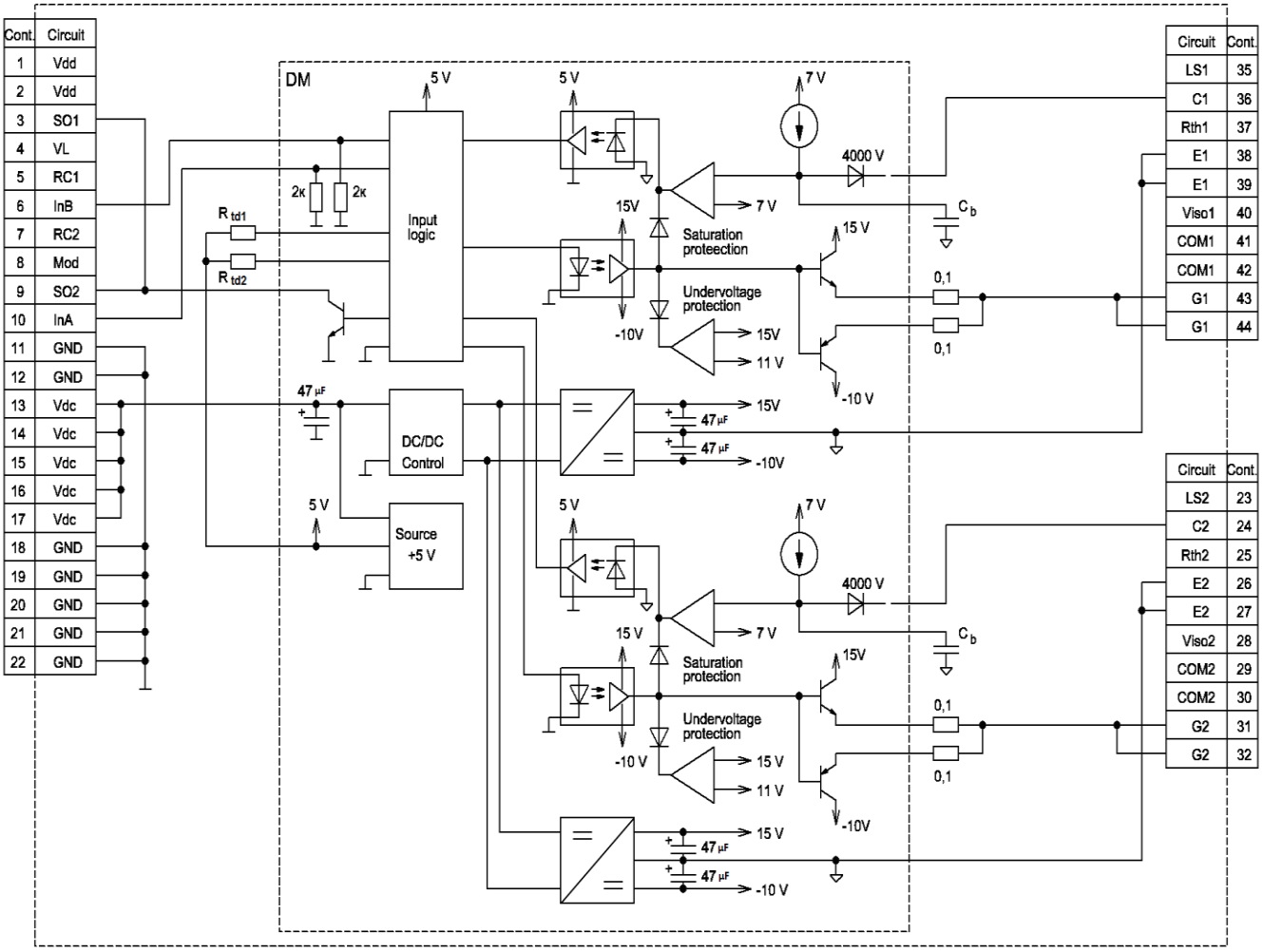


Figure 2– Functional driver circuit and turn-on circuit

3.3 Output function is given in Table 1.

Table 1 – Output function

Output No.	Function	Symbol
1	-	Not involved
2	-	Not involved
3	SO1	Error output (open collector)
4	-	Not involved
5	-	Not involved
6	INb	Controlled input of channel 2
7	-	Not involved
8	-	Not involved
9	SO2	Error output (open collector)
10	INa	Controlled input of channel 1
11	GND	Ground of control circuit and supply circuit
12	GND	Ground of control circuit and supply circuit
13	Vdc	Supply +15 V
14	Vdc	Supply +15 V
15	Vdc	Supply +15 V
16	Vdc	Supply +15 V
17	Vdc	Supply +15 V
18	GND	Ground of control circuit and supply circuit
19	GND	Ground of control circuit and supply circuit
20	GND	Ground of control circuit and supply circuit
21	GND	Ground of control circuit and supply circuit
22	GND	Ground of control circuit and supply circuit
23	-	Not involved
24	C2	Collector (drain) connection output of controlled transistor of channel 2
25	-	Not involved
26	E2	Emitter (source) connection output of controlled transistor of channel 2
27	E2	Emitter (source) connection output of controlled transistor of channel 2
28	-	Not involved
29	-	Not involved
30	-	Not involved
31	G2	Gate connection output of controlled transistor of channel 2
32	G2	Gate connection output of controlled transistor of channel 2
33	-	Not involved
34	-	Not involved
35	-	Not involved
36	C1	Collector (drain) connection output of controlled transistor of channel 1
37	-	Not involved
38	E1	Emitter (source) connection output of controlled transistor of channel 1
39	E1	Emitter (source) connection output of controlled transistor of channel 1
40	-	Not involved
41	-	Not involved
42	-	Not involved
43	G1	Gate connection output of controlled transistor of channel 1
44	G1	Gate connection output of controlled transistor of channel 1

4 BASIC AND MAXIMUM PERMISSIBLE PARAMETERS

Table 2 – Basic and maximum permissible parameters (at T = 25 °C)

Parameter	Symbol	Unit	Rate			Note
			min	type	max	
DC/DC block characteristic						
Supply voltage	U_S	V	13.5	15	16.5	
Off-load current consumption	I_S	mA		80	120	F_{cont} = 0 Hz
Maximum current consumption	$I_{S\ max}$	mA			550	Under load Ref. to Figures 5 and 6
Power of built-in power supply of output part	P_{DC-DC}	W	3			For each channel
Voltage monitor characteristics						
Turn-on threshold	U_{UVLO-}	V		11		DC-DC output
Turn-off threshold	U_{UVLO+}	V		12		
Control input characteristics						
High level intput voltage	U_{IH}	V	3	5	5.6	
Low level intput voltage	U_{IL}	V	-0.6	0	0.8	
Input resistance	R_{IN}	kΩ		2		
Time characteristics						
Turn-on/off delay time input-output	td (in-out)	μs			0.5	ref. to Figure 11
«Dead time» between signal changes of the first and second output channel	t_{TD}	μs	2			Set by consumer; ref. to Figure 10
Maximum operating frequency	f_{max}	kHz			100	No-load; ref. to Figure 5 and 6
Non-saturation protection operation delay time	t_{BLOCK1}	μs	2			Set by consumer; ref. to Figure 9
Lock time of controlled transistor after “Emergency”	t_{BLOCK2}	ms		70		
Soft emergency shutdown time of controlled transistor	toff	μs		1.5		
Emergency turn-on delay time	$td_{(on-err)}$	μs			2	
Output characteristics						
High level output voltage	U_{OH}	V	+12	+15	+18	In all range of permissible loads
Low level output voltage	U_{OL}	V	-8	-10	-12	
Maximum output pulse on current	$I_{Omax\ on}$	A	+18	20		Set by consumer; ref. to Figure 8
Maximum output pulse off current	$I_{Omax\ off}$	A		-22	-18	
Average output current	I_O	mA			130	To each channel
Rise and fall time of output signal	$t_{r\ (f)}$	ns			150	ref. to Figure 11
Maximum current of “Emergency” output	$I_{ERR\ max}$	mA			20	
Maximum voltage of “Emergency” output	$U_{ERR\ max}$	V			20	
Residual voltage of “Emergency” output	$U_{O\ ERR}$	V		0.3	0.7	at I_{ERR} = 20 mA
Saturation voltage that corresponds to non-saturation protection operation	U_{ms}^{Th}	V			6.0	at installing additional diodes – up to 4000 V
Insulation characteristics						
Maximum permissible reverse collector voltage	U_C	V			1000	
Insulations voltage between input	$U_{ISO(IN-OUT)}$	V			7500	DC, 1 minute

and output						
Insulation voltage between outputs of the first and second channel	$U_{ISO(OUT1-OUT2)}$	V			4000	DC, 1 minute
Critical rate of output voltage change	$(dU/dt)_{cr}$	kV/ μs			20	
Characteristics of controlled transistor						
Maximum permissible voltage of controlled transistor	U_{CE} (U_{DS})	V			3300	at installing additional diodes
Service and storage characteristics						
Operating temperature range	T_A	°C	-45		+85	
Storing temperature	Ts	°C	-60		+100	

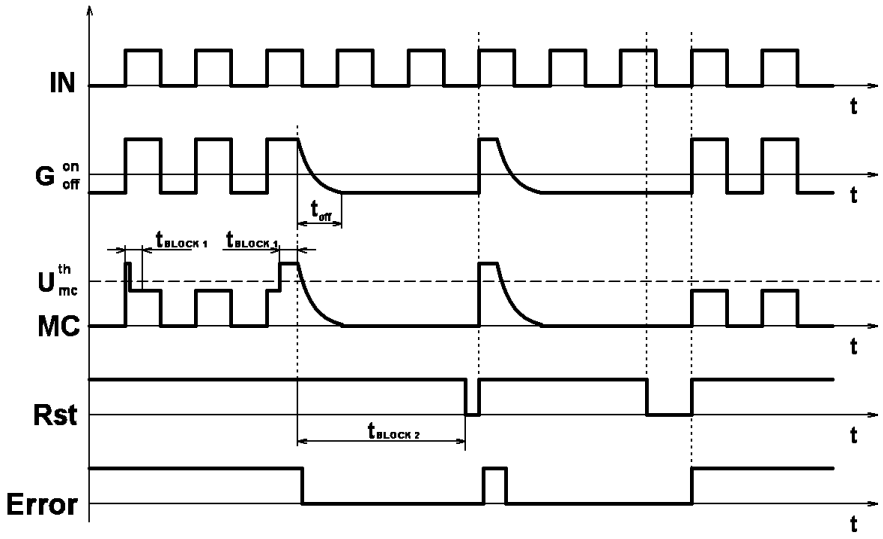
5 DRIVER OPERATION

Delivery of «log.1» on controlling input «INa» or «INb» will lead to opening of controlled transistor. Open state voltage fall increasing by more than U_{ms}^{Th} per time, exceeding t_{BLOCK1}, will lead to protection operation of open state voltage fall increasing (non-saturation protection). When "emergency" the transistor connected in accordance with the circuit with open collector («SO1» и «SO2») will open. In 70 ms emergency reset will be performed by internal circuit of emergency reset and on rising edge of control signal «IN» the controlled transistor will be opened. In the event when the emergency cause was not disposed then the protection cycle will be recurred.

Driver supply voltage decrease to protection operation threshold level against driver supply undervoltage «Uuvlo-» will lead to closing of controlled transistor regardless of input control signals. Control signals will recover on protection operation threshold against driver supply undervoltage «Uuvlo+». There is not an error signal on «SO» output when protection operation against supply undervoltage.

Simultaneous delivery of "log. 1" to outputs «INa» and «INb» will lead to control block and controlled transistors will be closed, thereby error signaling on «SO» output does not arise.

Diagrams explaining driver operation is shown at Figures 3 and 4.



Rst – Periodical internal signal of "emergency" reset

Figure 3 – Functional diagram of driver operation when «emergency»

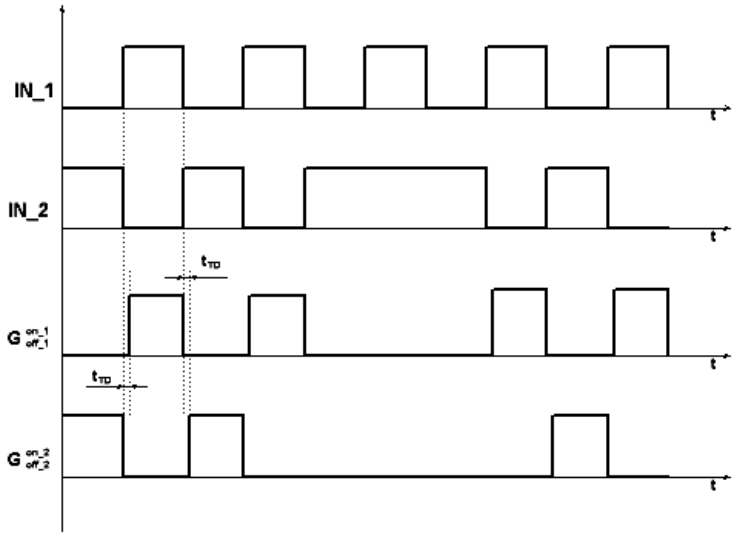


Figure 4 – Functional diagram of driver operation

6 DRIVER CONNECTION RECOMENDATIONS

INa, INb – controlling input. Driver control is described in section «Driver operation». When delivering of controlling voltage you must note that the protective reverse diodes are installed on control inputs. As result if control voltage exceeds supply voltage by more than 0.6 V then current consumption on inputs will be increased and with considerable increase of supply voltage the driver can fail. If the driver should be controlled by the level «log.1» of amplitude 15 V then it is recommended to connect the resistors 3.9…4.3 kΩ serially.

SO1, SO2 – outputs signaling about emergency. The outputs are transistor with open collector of protection circuit. Therewith transistor will open only when emergency caused by current overload of power transistor; if driver supply voltage is decreased to level «Uuvlo-» the transistors will be closed regardless of input control signals (signals will be recovered when reaching of supply level that corresponds to «Uuvlo+»), but "Error" signaling in this case will not occur. There won't be alarm too when simultaneous delivering of signals corresponding to «log.1» to controlled inputs, though output transistor will be closed.

It is not recommended to deliver to these outputs the voltage and current which values are higher than the maximum permissible including short-time.

Vdc – driver supply input. You should note that when driver supply voltage decrease, the output voltage of DC/DC – converter will be also decreased. Therewith if the supply is lower than the permissible level the input circuit can operate regularly but the voltage on gates of controlled transistor can drop to level «Uuvlo-» and transistor control will be false.

Maximum no-load current consumption on supply input is 120 mA. When transistors connecting the current consumption will increase by value of gate recharge current and can reach 550 mA (equal load to both channel). At higher current consumption DC/DC – converter can fail, or, on short-time current consumption increasing by 550 mA, output voltage of DC/DC – converter will decrease to unallowable level and undervoltage protection will operate, that will lead to faulty transistor drive. If the channel load is assigned irregularly then current consumption by one channel should not exceed 250 mA. Current consumption depends on control signal frequency, gate capacitance and gate resistors values as well as on input gate capacitance (ref. to Figure 6). Thereby, when using the driver you must make a correction for current consumption subject to transistors which the driver will work on. Safe operation area of the driver versus gate capacitance and frequency is shown at Figure 5.

GND – ground of control circuits and supply circuits; thereby control circuit is not galvanic disconnected with DC/DC-converter input.

Resistors Rtd1, **Rtd2** – timing resistor of switching delay setting of the first and second channel. Actually resistors regulate turn-on delay time thereby when installing the resistor of diverse nominal the switching delay of leading edge of controlled pulses of the first and second channel will be different.

If there is no need for increasing of switching delay time, then you shall install the jumpers instead of resistors. The dependence of delay time on the resistor nominal is shown at Figure 10. Initially the resistors of 1 Ω nominal are installed that corresponds to minimum "dead time" (2μs).

Capacitor C_{b1} , C_{b2} – timing turn-off delay capacitor of corresponding controlled transistor at current overload. Protection operation delay is necessary to avoid the false operation of short-time inductive kicks and of turn-on transient process. Thereby the delay duration will be equal to "rerun pulse" duration in case of emergency. To increase protection operation delay you are recommended to adjust capacitors with nominal shown at Figure 9. Initially the capacitors of 100 pF capacitance are set that corresponds to delay time 5μs (typ.).

G1, G2 – outputs meant for gates connection of controlled transistors.

Gate resistors' adjustment is recommended, they are necessary for maximum pulse current decrease. Resistor adjust of every nominal including 0 Ω is allowed. Resistor adjustment with different nominal is also allowed (serially to diode), for instance, in order that to increase turn-on time of controlled transistor purposely to decrease voltage amplitude of inductive kicks. Output pulse current versus gate resistor nominal is shown at Figure 8.

C1, C2 – collector (drain) connection output of controlled transistor. The outputs are intended for voltage fall controlling (non-saturation protection) on transistor. To increase the operating voltage up to 4000 V it is necessary to install in series three diodes of type HER108 or by similar parameters, by anode to output C1(C2). Thereby maximum value of protection operation threshold is 5.0 V.

If there is no need for current overload protection then the output «C» should be short-circuited to emitter output of corresponding channel.

E1, E2 – emitter connection outputs of controlled transistor.

7 GRAPHS EXPLAINING DRIVER OPERATION

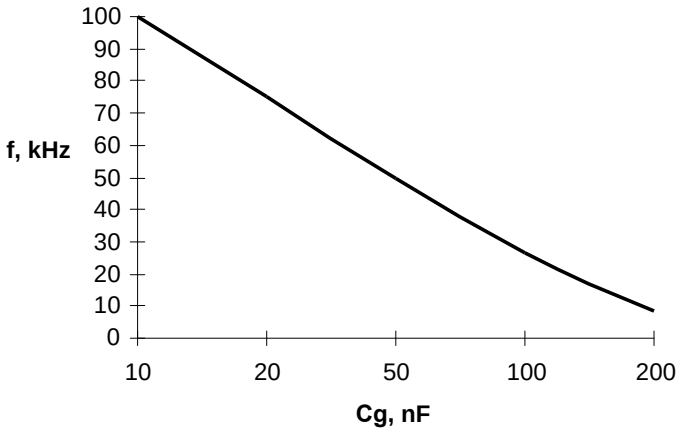


Figure 5 – Safe operation area versus frequency and gate capacitance (with gate resistor 1 Ω)

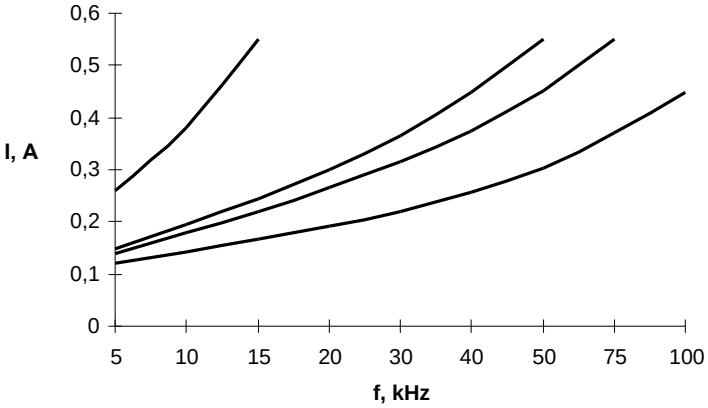


Figure 6 – Current consumption versus signal frequency under load (with gate resistor 1 Ω)
For gate capacitance 10 nF, 25 nF, 50 nF, 100 nF

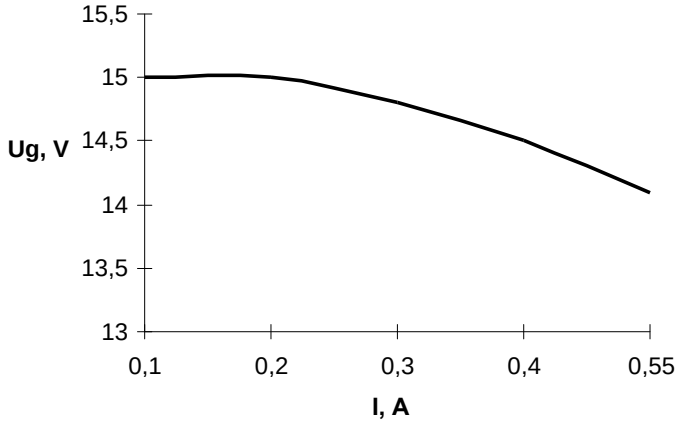


Figure 7 –Transistor gate voltage versus current consumption

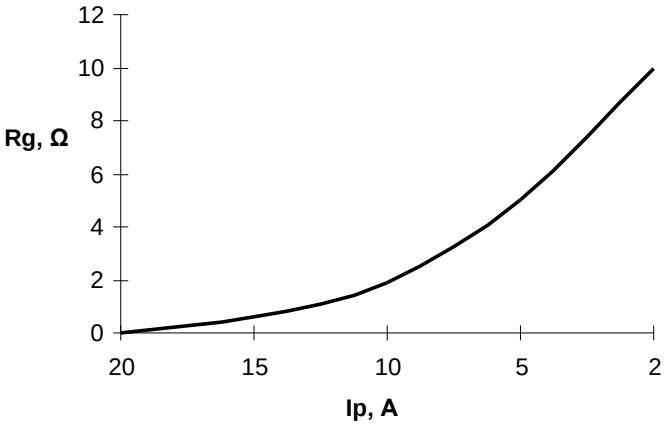


Figure 8 – Output pulse current versus gate resistor nominal

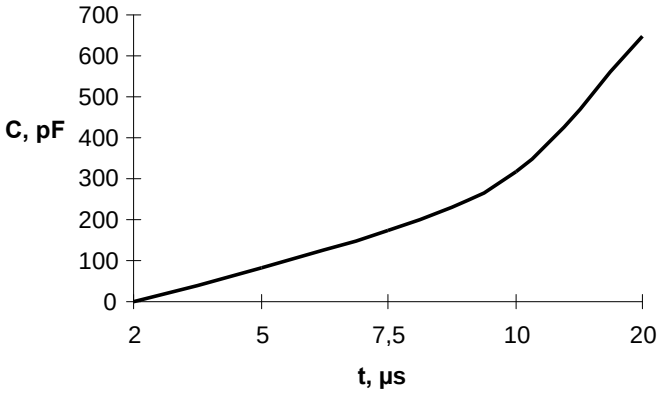


Figure 9 – Turn-on delay time of saturation voltage versus trimming capacitance C_b nominal

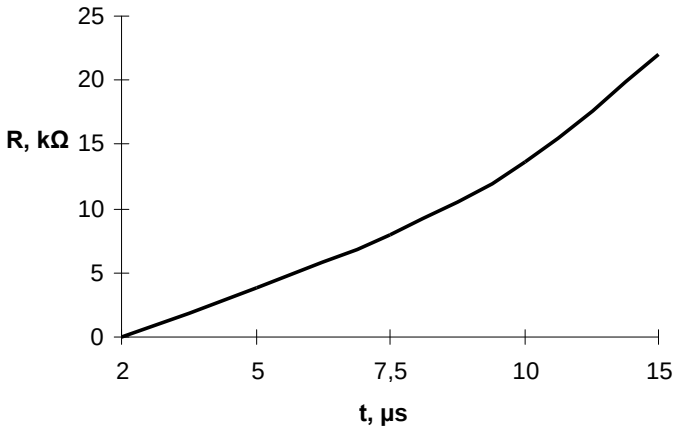


Figure 10 – "Dead time" duration versus trimming resistor R_{TD} nominal

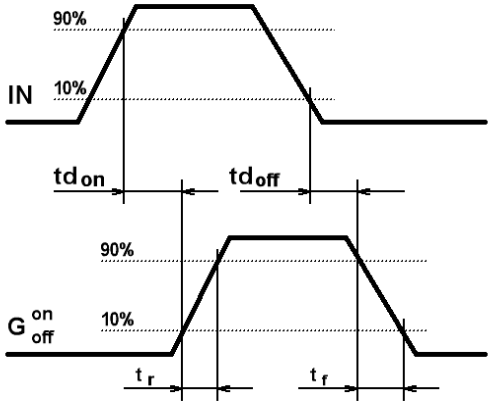


Figure 11 – Diagram explaining timing driver characteristics
where IN – input control signal; G – gate signal of controlled transistor

8 INFORMATION ABOUT PRECIOUS METALS

Precious metals are not contained.

9 SERVICE RECOMMENDATIONS

9.1 Resistance requirements at mechanical impacts

Mechanical impacts for drivers in accordance with qualifying standards of controlled power transistors are shown in Table 3.

Table 3 – Drivers resistance requirements to mechanical impact factors

External exposure factors	External exposure factor value
Sinusoidal vibration:	
- frequency range, Hz;	0.5 - 100
- acceleration amplitude, m/s^2 (g)	150 (15)
Mechanical shock of single action:	
- peak shock acceleration, m/s^2 (g);	40 (4)
- pulse duration of shock acceleration, ms	50

9.2 Resistance requirements at climatic impacts

Table 4 - Resistance requirements to climatic impact factors

Climatic factor	Climatic factor value
Lower ambient temperature:	
- operating, °C;	minus 45
- maximum, °C	minus 60
Higher ambient temperature:	
- operating, °C;	+85
- maximum, °C	+100
Relative humidity with temperature 35 °C without moisture condensation, %, max	98
Ambient temperature change, °C	from minus 60 to +100
Lower atmospheric pressure, Pa (mm Hg)	86000 (650)
Higher atmospheric pressure, Pa (mm Hg)	106000 (800)

10 RELIABILITY SPECIFICATIONS

Reliability probability of drivers for 25000 hours must be at least 0.95.

Gamma-percent life must be no less than 50000 hours by $\gamma = 90$ %.

Gamma-percent service life of the modules, subject to cumulative operating time is no more than gamma-percent life, no less than10 years, at $\gamma = 90$ %.

Gamma-percent storageability time of the modules, at $\gamma = 90$ % and storing – 10 years.

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